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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/763,554	01/23/2004	Hirokazu Honda	NEC 26485	7561

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EXAMINER	
WILLIAMS, ALEXANDER O	
ART UNIT	**PAPER NUMBER**
2826	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/763,554	HONDA, HIROKAZU	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *10-15,18 and 19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-9,16 and 17* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Serial Number: 10/763554 Attorney's Docket #: NEC 26485
Filing Date: 1/23/2004; priority to 2/3/2003 and 12/10/2003

Applicant: Honda

Examiner: Alexander Williams

Applicant's Amendment filed 4/20/07 to the election of the species I, figures 1a, 1b, 8a-8h and 12a (claims 1-9, 16-18 and 19), filed 9/26/05, has been acknowledged. As of this action, claims 18 and 19 are now withdrawn.

This application contains claims 10-15, 18 and 19 drawn to an invention non-elected without traverse.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4 and 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Attarwala (U.S. Patent Application Publication #2004/0195701 A1).

1. Attarwala (figures 1 to 26) specifically figures 2 and 7 show a semiconductor device comprising: a semiconductor chip **36** mounted on a mounting substrate **122**; a first resin **32** filling a gap between the semiconductor chip and the mounting substrate; a stiffener **126** surrounding the semiconductor chip; and a second resin **36** filling a space between the semiconductor chip and the stiffener in contact with the first resin, the first resin being different **(being different is interpret to means not the other)** in a thermal expansion coefficient from the second resin (see figure 7).

4. The semiconductor device as claimed in claim 1, Attarwala show wherein the first resin includes an underfill **32** part filling the gap between the semiconductor chip and the mounting substrate, and a fillet part extended from a region of the semiconductor chip.

6. The semiconductor device as claimed in claim 4, Attarwala show wherein the second resin **36** is in contact with inner walls of the stiffener **26**, the fillet part **32**, the mounting substrate **22** and each of side faces of the semiconductor chip **30**.

[0090] Referring to FIG. 2, chip 30 is secured to support member 22 of electronic package substrate 20, electrically connected to circuitized member 26, and protected from the environment, using conventional materials. Die attach adhesive 32, used to attach chip 30 to support member 22 of electronic package substrate 20, is a thermally conductive, dielectric adhesive, preferably a thermally conductive, dielectric epoxy. Wire bonds 34, which connect chip 30 to circuitized member 26, are electrical conductors, preferably gold wires. Encapsulant 36, which covers or encapsulates chip 30 and wire bonds 34, is preferably an epoxy resin compound; however any non-reactive, non-conductive material that provides mechanical integrity would be satisfactory.

Initially, it is noted that the 35 U.S.C. § 103 rejection based on a second resin, a stiffener and (an adhesive or first adhesive) deals with an issue (i.e., the integration of multiple pieces into one piece or conversely, using multiple pieces in replacing a single piece) that has been previously decided by the courts.

In Howard v. Detroit Stove Works 150 U.S. 164 (1893), the Court held, "it involves no invention to cast in one piece an article which has formerly been cast in two pieces and put together...."

In In re Larson 144 USPQ 347 (CCPA 1965), the term "integral" did not define over a multi-piece structure secured as a single unit. More importantly, the court went further and stated, "we are inclined to agree with the solicitor that the use of a one-piece construction instead of the [multi-piece] structure disclosed in Tuttle et al. would be merely a matter of obvious engineering choice" (bracketed material added). The court cited In re Fridolph for support.

In re Fridolph 135 USPQ 319 (CCPA 1962) deals with submitted affidavits relating to this issue. The underlying issue in In re Fridolph was related to the end result of making a multi-piece structure into a one-piece structure. Generally, favorable patentable weight was accorded if the one-piece structure yielded results not expected from the modification of the two-piece structure into a single piece structure.

Claims 1 to 4, 6 to 9, 16 and 17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Caletka et al. (U.S. Patent # 6,410,988 B1).

1. Caletka et al. (figures 1 to 7) specifically figures 4 and 5 show a semiconductor device **10** comprising: a semiconductor chip **12** mounted on a mounting substrate **16**; a first resin **17** filling a gap between the semiconductor chip and the mounting substrate; a stiffener **(outer portion of 26)** surrounding the semiconductor

chip; and a second resin **(inner portion of 26)** filling a space between the semiconductor chip and the stiffener in contact with the first resin, the first resin being different in a thermal expansion coefficient from the second resin.

(5) A method of forming flip chip package 10 comprises providing chip 12 and laminate substrate 16 and attaching electrical contacts of chip 12 on active surface 15 to circuitry of laminate substrate 16 preferably by a heating cycle to form solder interconnections. Chip 12 is comprised of materials well known in the art. An exemplary list of materials includes silicon, germanium and gallium arsenide. Laminate substrate 16 is typically a laminated circuit board having a number of electrical circuits defined within and is adapted for interconnection with other components of an electronic assembly. Laminate substrate 16 is comprised of materials well known in the art, for example, polyimide, polytetrafluoroethylene and liquid crystal polymer. A suitable material, for example, is an epoxy glass composite commercially available as DriClad.RTM. from IBM Corporation. Preferably, underfill material 17 is applied between the connected contacts of chip 12 and laminate substrate 16. **The underfill material is typically an electrically non-conductive coupling material, for example, a filled epoxy. A suitable filled epoxy is commercially available as HYSOL.RTM. 4511 from Dexter Corporation.** Underfill material 17 acts as a buffer for stresses that arise due to the differences between the CTE of the chip and the laminate substrate, and it also serves to protect the soldered connections from moisture. **The underfill material may extend past periphery 20 of chip 12.**

1. (6) The thermally enhanced flip chip package also comprises body 26. **FIG. 4 shows body 26 is preferably applied to upper surface 18 and around periphery 20 of chip 12. Body 26 is preferably applied as an uncured dielectric material, and a suitable material is an epoxy commercially available as Masterbond Supreme 10AOHT from the Masterbond Corporation.** Body 26 may be applied in any configuration and preferably a pattern, for example a substantially "X" shaped pattern, that minimizes trapped air when body 26 is subsequently displaced. Body 26 may be applied to chip 12 or to laminate substrate 16 or to thermally conductive member 22 or combinations thereof. Body 26 is preferably applied at a temperature range between about 20.degree. C. to about 28.degree. C.

(7) Underfill material 17 may be uncured or partially uncured before body 26 is applied. If underfill material 17 is cured prior to application of body 26, the surface of underfill material is treated to promote adhesion to body 26.

Preferably, underfill material 17 undergoes a surface treatment, and preferably plasma etch, at the surface of the underfill material where it comes into contact with body 26.

(9) After thermally conductive member 22 is contacted with **body 26, preferably an uncured dielectric material**, the body is cured. The temperature and time for curing vary with the type of material used for the body. **For example, Masterbond Supreme 10AOHT epoxy from Masterbond Corporation is preferably cured for about one hour at a temperature of about 130.degree. C.** It is preferable that the cure temperature of body 26 is approximately equal to the gel temperature of underfill material 17 to produce a flip chip package that is nearly stress free during cure, however, it is preferable that the underfill material is cured before the body is applied. When body 26 is cured, it is in intimate bonded contact with thermally conductive member 22, flip chip 12, and laminate substrate 16. Body 26 effectively encapsulates flip chip 12.

2. The semiconductor device as claimed in claim 1, Caletka et al. show wherein a thermal expansion coefficient of the second resin **26** is smaller than a thermal expansion coefficient of the first resin **17**.

3. The semiconductor device as claimed in claim 2, Caletka et al. show wherein the stiffener is adhered to the mounting substrate **16** with a resin **26** the same as the second resin **26**.

4. The semiconductor device as claimed in claim 1, Caletka et al. show wherein the first resin **17** includes an underfill part filling the gap between the semiconductor chip **12** and the mounting substrate **16**, and a fillet part **(extending portion of**

17 not directly under 12) extended from a region of the semiconductor chip.

6. The semiconductor device as claimed in claim 4, Caletka et al. show wherein the second resin **(inside portion of 26)** is in contact with inner walls of the stiffener **(outer portion of 26)**, the fillet part **(extending portion of 17 not directly under 12)** the mounting substrate **16** and each of side faces of the semiconductor chip **12**.

7. Caletka et al. (figures 1 to 7) specifically figures 4 and 5 show a semiconductor device **10** comprising: a semiconductor chip **12** mounted on a mounting substrate **16**; a first resin **17** filling a gap between the semiconductor chip and the mounting substrate; a stiffener **(outer portion of 26)** surrounding the semiconductor chip; a second resin **(inner portion of 26)** filling a space between the semiconductor chip and the stiffener in contact with the first resin, the first resin being different in a thermal expansion coefficient from the second resin; and a lid **22** for covering the stiffener and the semiconductor chip, wherein the lid is bonded to the stiffener and a backside of the semiconductor chip with an adhesive **(26 portion between 22 and 12)**.

8. The semiconductor device as claimed in claim 7, Caletka et al. show wherein the second resin **26** is in contact with an inner wall of the lid.

9. The semiconductor device as claimed in claim 1, Caletka et al. show wherein an elastic modulus of the second resin **26** is larger than an elastic modulus of the first resin **17**.

16. The semiconductor device as claimed in claim 1, Caletka et al. show wherein the stiffener **(outer portion of 26)** is made of a material selected from the group consisting of Cu, SUS, Al, alumina, silicon, aluminum nitride, and **resin**.

17. The semiconductor device as claimed in claim 1, Caletka et al. show wherein each of the first resin **17** and the second resin **26**essentially contains a resin selected from a group consisting of **epoxy**, polyolefin, silicon, cyanate ester, polyimide, polynorbornene resins.

Therefore, it would have been obvious to one of ordinary skill in the art to use the second resin, the stiffener and the second adhesive as "merely a matter of obvious engineering choice" as set forth in the above case law.

Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response

Applicant's arguments filed 4/20/07 have been fully considered, but are not found to be persuasive in with respect to Caletka et al. and in view of the new grounds of rejections detailed above.

Applicant states that Caletka et al. does not show "the first resin being different in a thermal expansion coefficient from the second resin." However, to prove that Caletka et al. has a difference thermal expansion coefficient in the first and second resin to just to show that the first resin and the second resin are different. Caletka et al. show that the first and second resin are different.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/778,737,738,734,787,788,789,790,795,792,793,796,704,706,707,710,712,713,717,720,698,783,e23.14,e23.092,23.087,e23.19,e23.069,e23.101,e23.007	10/13/05 5/11/06 12/6/06 7/1/07
Other Documentation: foreign patents and literature in 257/778,737,738,734,787,788,789,790,795,792,793,796,704,706,707,710,712,713,717,720,698,783,e23.14,e23.092,23.087,e23.19,e23.069,e23.101,e23.007	10/13/05 5/11/06 12/6/06 7/1/07
Electronic data base(s): U.S. Patents EAST	10/13/05 5/11/06 12/6/06 7/1/07

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
7/1/07